IN THE CLAIMS

Please amend the claims as follows.

1. (Previously Presented) A circuit comprising:

a reference current source to provide a substantially noise free differential current signal; and

a detector coupled to one or two power supplies, the detector to receive the substantially noise free differential current signal, to detect a noise signal on the one power supply or the two power supplies, and to generate a high noise detection signal to indicate detection of the noise signal.

2. (Previously Presented) A circuit comprising:

a reference current source to provide a substantially noise free differential current signal; and

a detector coupled to one or two power supplies, the detector to receive the substantially noise free differential current signal, to detect a noise signal on the one power supply or the two power supplies, and to generate a high noise detection signal to indicate detection of the noise signal;

wherein the detector comprises:

a PMOS current mirror to receive the substantially noise free differential current signal;

an NMOS current mirror to receive a substantially noise free complementary current signal;

a first resistor coupled to the PMOS current mirror;

a second resistor coupled to the NMOS current mirror;

a comparator coupled to the current mirrors and the resistors;

two resistor-capacitor high-pass filters, each coupled to one of the two comparator's inputs;

one or more capacitors, each of the one or more capacitors coupled to at least one of the two power supplies and to a resistor-capacitor high-pass filter via a NMOS switch;

a filter load, comprising selectable low-pass filter paths, each path comprising pass-gates and a resistor-capacitor low-pass filter, the filter load is coupled to the comparator;

a Schmitt trigger coupled to the filter load, the Schmitt trigger to generate the pre-noise detection signal;

an exclusive-OR gate coupled to the Schmitt trigger, to provide noise polarity selection;

a logic-high latch comprising a NOR gate, a NAND gate, and three inverters, to store the high noise detection signal, and to reset the high noise detection signal; and

a flip-flop register coupled to the logic-high latch to synchronize the high noise detection signal.

3. (Previously Presented) A circuit comprising:

a reference current source to provide a substantially noise free differential current signal; and

a detector coupled to one or two power supplies, the detector to receive the substantially noise free differential current signal, to detect a noise signal on the one power supply or the two power supplies, and to generate a high noise detection signal to indicate detection of the noise signal;

wherein the reference current source comprises:

a substantially noise free ground;

a control signal source;

a voltage reference coupled to the substantially noise free ground;

a voltage follower differential amplifier coupled to the substantially noise free ground and to the voltage reference;

a PMOS-NMOS-NMOS diode stack coupled to the voltage follower differential amplifier and to the substantially noise free ground;

Controllable NMOS current scalers coupled to the substantially noise free ground signal source, the control signal source, and the diode stack, and a PMOS transistor load, to provide a calibration voltage for controllable PMOS current scalers;

NMOS current mirrors coupled to the controllable PMOS current scalers and the substantially noise free ground to provide the substantially noise free reference current signal; and

PMOS current mirrors coupled to a NMOS current mirrors, and the substantially noise free ground, to provide the substantially noise free complementary reference current signal.

4. (Original) The circuit of claim 3, wherein the voltage reference comprises a bandgap voltage reference.

5. (Original) A circuit comprising:

a plurality of reference current sources formed on a substrate, each of the plurality of reference current sources to provide a substantially noise free differential current signal; and

a plurality of detectors formed on the substrate, each of the plurality of detectors coupled to one or two power supplies, each of the plurality of detectors to receive the substantially noise free differential current signal and to detect a noise signal on the one or two power supplies and to generate a noise detection signal to indicate detection of the noise signal.

6. (Original) The circuit of claim 5, wherein the substrate comprises silicon.

7. (Original) The circuit of claim 6, wherein each of the plurality of detectors comprises a comparator.

8. (Original) The circuit of claim 7, wherein each of the comparators comprises complementary metal-oxide semiconductor field-effect transistors.

9. (Original) The circuit of claim 5, wherein the substrate comprises gallium arsenide.

10. (Original) The circuit of claim 6, wherein each of the plurality of reference current sources comprises a pair of complementary current sources.

11. (Original) The circuit of claim 5, wherein the substrate comprises silicon and germanium.

12. (Original) The circuit of claim 11, wherein each of the plurality of reference current sources comprises a controllable current source.

13. (Original) The circuit of claim 5, wherein the substrate comprises a processor.

14. (Original) The circuit of claim 13, wherein the processor comprises a very-long instruction word processor.

15. (Currently Amended) A method comprising:

producing a substantially noise free <u>differential</u> current signal<u>, wherein a first current signal of the substantially noise free differential current signal is provided by a PMOS current mirror, and a second current signal of the substantially noise free differential current signal is provided by an NMOS current mirror;</u>

detecting one or two power supply signals;

processing the substantially noise free current signal and the one or two power supply signals to detect a noise signal in the one or two power supply signals; and

generating a noise detection signal in response to detection of the noise signal.

16. (Previously Presented) A method comprising:

receiving a substantially noise free current signal;

receiving one or two power supply signals;

processing the substantially noise free current signal and the one or two power supply signals to detect a noise signal in the one or two power supply signals; and

generating a noise detection signal in response to detection of the noise signal;

wherein receiving the substantially noise free current signal comprises:

receiving a pair of complementary current signals.

17. (Original) The method of claim 15, wherein receiving the one or two power supply signals comprises:

receiving two voltage signals having different polarities.

18. (Original) The method of claim 15, wherein processing the substantially noise free current signal and the one or two power supply signals to detect the noise signal in the one or two power supply signals comprises:

comparing the one or two power supply signals to the substantially noise free current signal.

19. (Original) The method of claim 15, wherein generating the noise detection signal in response to detection of the noise signal comprises:

generating a digital signal in response to detection of the noise signal.

20. (Original) The method of claim 15, further comprising:

setting a calibration potential level; and

setting a noise-detection threshold level.

21. (Previously Presented) The circuit of claim 1, wherein the reference current source comprises a controllable current source.

22. (Previously Presented) The circuit of claim 2, wherein the reference current source comprises a controllable current source.

23. (New) The method of claim 16, wherein processing the substantially noise free current signal and the one or two power supply signals to detect the noise signal in the one or two power supply signals comprises:

comparing the one or two power supply signals to the substantially noise free current signal.